

REMARKS

Claims 1 to 10 were pending in the application at the time of examination. Claims 1 to 10 stand rejected as anticipated.

Claims 1 to 10 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,038,663, hereinafter referred to as Feldman.

Applicants respectfully traverse the anticipation rejection of Claim 1.

The Office Action copied the body of Claim 1, then cited to Column 23, lines 1 - 33 of Feldman as disclosing Claim 1.

Applicants point out that to support an anticipation rejection, the MPEP requires:

"The identical invention must be shown in as complete detail as is contained in the ... claim." . . . The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required.

MPEP, §2101, 8th Ed., Rev. 2, p. 2100-120 (May 2004).

As discussed more completely below, the foregoing cited part of Feldman must show the identical invention in as complete detail as is contained in Claim 1.

The cited section of Feldman discloses an initialization and operation mode determination of a power on self test (POST) initialization sequence of a module of the invention.

According to part of the cited section of Feldman:

A test is performed to determine whether to use the BIOS in flash memory or in ROM. Pin BDIS- (pin 219) in the embodiment represent in Table 10) is tested. In one embodiment, if BDIS- is pulled low, e.g. connected to ground by an external jumper, then the BIOS is obtained from ROM, and, if BDIS- is allowed to float or pulled high, then the BIOS is obtained from flash memory. . . . If BIOS in the flash memory should become corrupted, BDIS- may be set to use the BIOS in ROM, and a serial connector configured (as described below) to place the module in a

download configuration may be connected to a serial port.

Claim 1 recites in part:

...decoding, by said processor, said message to
determine the execution mode of the embedded device;

indicating, by said processor, code in said first
code space is corrupted if said execution mode indicates
said embedded device is executing in said second code
space; and

indicating, by said processor, said code in said
first code space is valid if said execution mode indicates
said embedded device is executing in said first code
space.

Applicants respectfully note that the rejection is silent
as to which specific portions of the cited section of Feldman
the Examiner alleges taught the elements of Claim 1. Despite
this, Applicants note that none of the cited section of Feldman
taught indicating by a processor that **code in said first code
space is corrupted if the execution mode indicates the embedded
device is executing in said second code space or that code in
the first code space is valid if the execution mode indicates
that the embedded device is executing in the first code space.**

If the Examiner equated "a test is to be performed to
determine whether to used the BIOS in flash memory or in ROM.
Pin BDIS- . . . is tested" with indicating if code in a first
code space is corrupted or valid, Applicants note that this
test of Feldman bears no relationship to either the type of
determination recited in Claim 1 or to the conditional
indications based on the outcome of the determination recited
in Claim 1.

With respect to the type of determination or test, the
cited section of Feldman explicitly taught that **the pin BDIS-
is tested for a type of signal; e.g., whether the signal is
floated, pulled high, or pulled low.** This has nothing to do
with the type of determination recited in Claim 1, which

recites that **a decoded message indicates whether code is executing in a first code space or a second code space.**

With respect to the indications resulting from the outcome of a determination or test, the cited section of Feldman explicitly taught that the specific outcome of its test was used to determine **whether to use BIOS in flash memory or ROM.** This taught nothing about the outcome of the determination recited in Claim 1; i.e., **whether the code in a first code space is valid or corrupted.**

Feldman failed to teach or describe a decoded message indicating whether code is executing in a first code space or a second code space, and further failed to teach or describe indicating if code in said first code space is corrupted by determining where code is executing. Thus, Feldman fails to show "[t]he identical invention . . . in as complete detail as is contained in the . . . claim." Therefore, according to the MPEP, Feldman fails to anticipate Claim 1. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of Claim 1.

Claims 2 and 3 depend from Claim 1 and so distinguish over Feldman for at least the same reasons as Claim 1. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 2 and 3.

With respect to the anticipation rejection of Claim 4, the Office Action gave the identical rejection as discussed above for Claim 1. Claim 4 is the means for performing the method of Claim 1 and so distinguishes over Feldman for the same reasons as Claim 1, and the remarks concerning Claim 1 are incorporated herein by reference. Applicants respectfully request reconsideration and withdrawal of the anticipation of Claim 4.

Claims 5 and 6 depend from Claim 4 and so distinguish over Feldman for at least the same reasons as Claim 4. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 5 and 6.

With respect to the anticipation rejection of Claim 7, Claim 7 includes limitations equivalent to those discussed above with respect to Claim 1 and the Office Action cited the same section of Feldman as teaching these limitations. Therefore, the above remarks with respect to Claim 1 are applicable to Claim 7 and are incorporated herein by reference.

Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of Claim 7.

Claim 8 and 9 depend from Claim 7 and so distinguish over Feldman for at least the same reasons as Claim 7. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of each of Claims 8 and 9.

With respect to the anticipation rejection of Claim 10, the Office Action again cited Feldman Column 23, lines 1 - 33.

Claim 10 recites in part:

...examining, by a processor, a message received from a remote device to determine an execution mode of said remote device...;

indicating validity of code in said first code space based on whether said execution mode indicates said remote device is executing in said second code space.

As discussed above with respect to Claim 1 and incorporated herein by reference, the cited section of Feldman taught nothing about **indicating whether code is executing in a second code space**, and taught nothing about **the validity of the code in a first code space**. Therefore, Feldman fails to anticipate Claim 10. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of Claim 10.

Claims 1 to 10 remain in the application. For the foregoing reasons, Applicant(s) respectfully request allowance of all pending claims. **If the Examiner decides not to allow the claims, Applicants respectfully request that the action is continued, and not made final, in view of the lack of**

interpretive comments for the cited sections, as heretofore discussed. Applicants further respectfully request that any future action include Examiner's interpretation of the cited reference(s), to permit Applicants an opportunity to respond to Examiner's rejections without conjecture on Applicants' part as to the Examiner's reasoning regarding any such findings.

Applicants appreciate Examiner's consideration in this matter.

If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 13, 2005

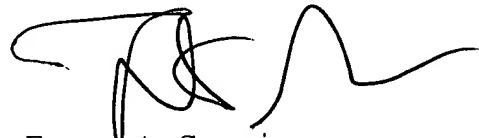
Respectfully submitted,



October 13, 2005

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Date of Signature



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